EXHIBIT 9

Williams Wireless Technologies et al.
v.
Research in Motion, et al.

Plaintiffs' Amended Disclosures Pursuant to Local Rule 3-1

Infringing Instrumentalities of:

Research In Motion Corporation

STATEMENT REGARDING ACCUSED

RIM WIRELESS COMMUNICATIONS PRODUCTS

The accompanying claim chart explains the basis for infringement of claims 1, 2, 3, 4, 6 and 7 of U.S. Patent No. 4,809,297 (the ‘297 Patent) by RIM’s wireless communications products. These bases apply to all of RIM’s presently identified products including the wireless mobile phones identified in the Complaint and hereinafter, which, for purposes of this action, are believed to be functionally equivalent from an infringement standpoint.

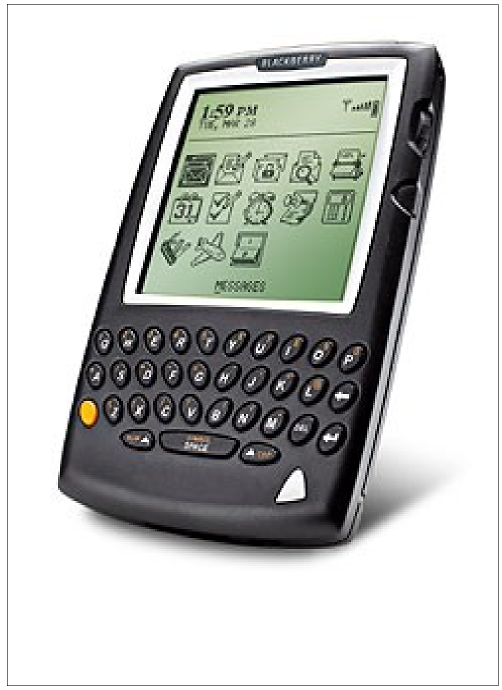
Williams Wireless Technologies and Polansky Electronics, Ltd. reserve the right to refine and improve the claim charts as discovery progresses and, in particular, after RIM provides full information regarding its products pursuant to Local Rule 3-4. In addition, Williams Wireless Technologies and Polansky Electronics, Ltd reserve the right to supplement the claim charts once they are provided with discovery regarding each of the RIM wireless communications devices named herein and have had an opportunity to obtain testimony on the accuses and suspected products from RIM.

Unless otherwise stated herein, the specified element of each asserted claim is believed to be literally present in the accused instrumentality.

Pursuant to Local Rule 3-1, and for each claim asserted hereinafter, Williams Wireless Technologies and Polansky Electronics, Ltd. identify the following:

Williams Electronics Limited F.M.I.D. Facsimile Mobile Interface Data Device Model R100-5767.

PDCharm Chipset



Several RIM devices, such as the 5790 device pictured to the right, include the PDCharm chipset from the Intel Corporation. The little publicly available information describing the particular functionality and inner details of the chipset are found in various Service Manuals and promotional materials. Representative schematic diagrams of the PDCharm chipset are reproduced in Appendix A and referred to throughout this analysis and claims chart. The PDCharm and other chipsets based on the Intel Xscale Technology include circuitry and componentry that causes the host device to interface a data transfer device with a radio transceiver, as claimed in U.S. Patent 4,809,297.

Plaintiff further alleges that other devices manufactured by RIM and other Defendants that incorporate the identified chipset also infringe in the same manner as detailed below. For the purpose of this Claim Chart, an "accused instrumentality" is any device of the Defendant that incorporates the features and functionality embodied in the PDCharm chipset or other chipsets based on the Xscale Technology.

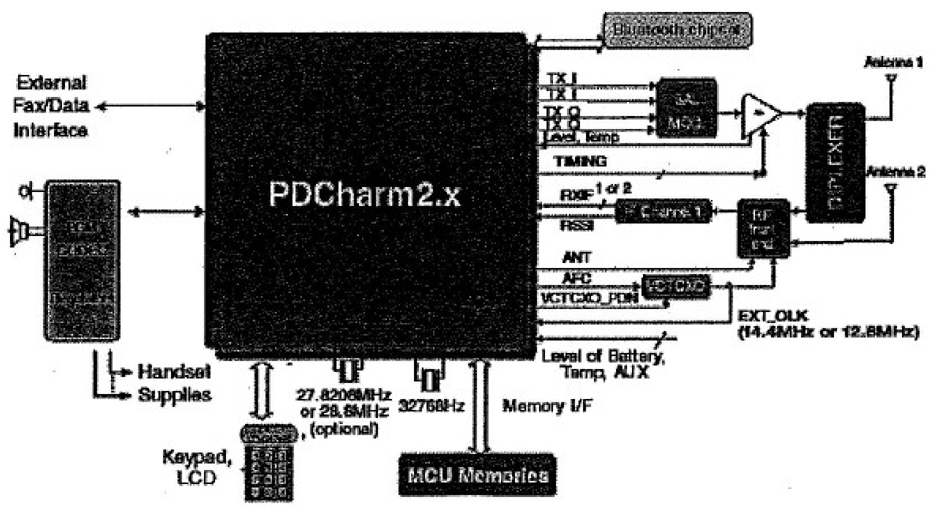
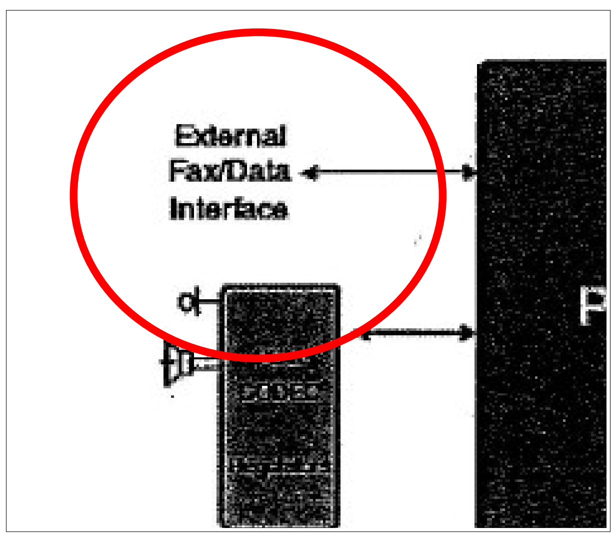


Figure 2: System Block Diagram of a typical handset design using PDCharm2.X

CLAIM CHART

1. An interface to connect a data transfer device with a radio transceiver *comprising:*	The accused device includes the chipset identified above, which is an interface to connect a data transfer device with a radio transceiver. The accused device includes several components, any one or more of which constitute a data transfer device. In one example, the accused device includes a keyboard (identified as "A") which is a data transfer device.  Other components coupled to the identified chipset may also constitute a "data transfer device", such as any one or more devices connected to the "External Fax/Data Interface" portion of the identified chipset below. Data Transfer Device 

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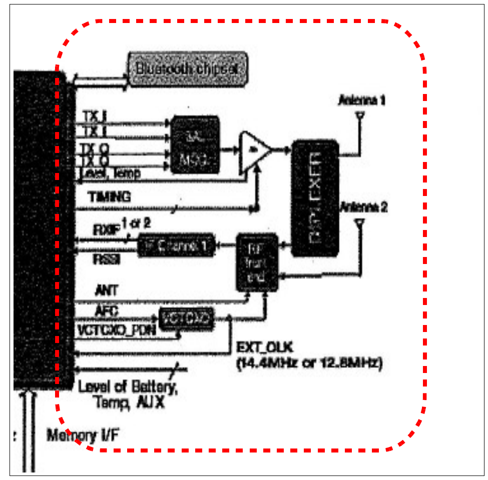
<td>The accused device further includes a radio transceiver as identified in the representative chipset diagram reproduced to the right. The components constituting the radio transceiver include the RF-part and the Bluetooth components.


Transceiver Portion of PDCharm chipset</td>
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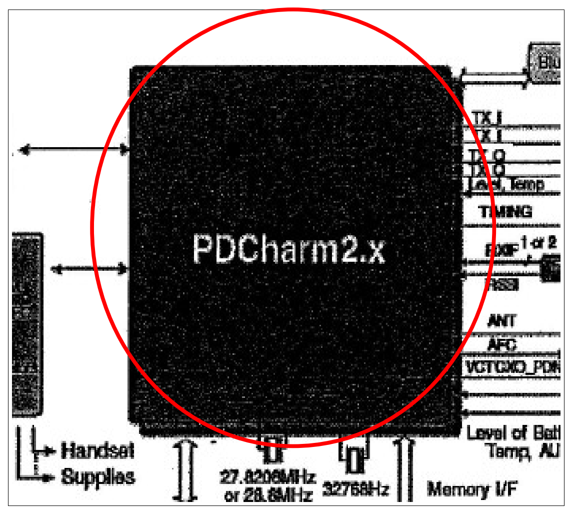
<td>a receiving circuit to receive a data signal in a given form from said transceiver,</td>
<td>The identified chipset embedded in the accused instrumentality includes a receiving circuit embedded within the component identified as the "Baseband Procesor" (the PDCHarm2.x). The Baseband Processor includes both a receiving circuit and a transmitting circuit, as is more evident with reference to the detailed schematic reproduced as "Schematic 1" in Appendix A.

The receiving circuit receives a data signal in a given form from the transceiver.

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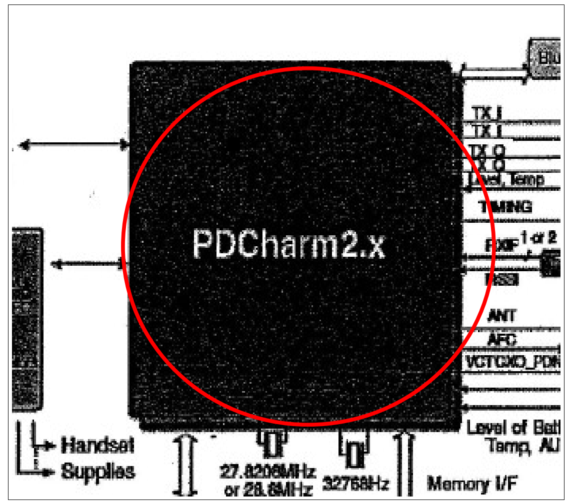
<td>a transmitting circuit to transmit a data signal in said given form to said transceiver,</td>
<td>The identified chipset embedded in the accused instrumentality includes a transmitting circuit embedded embedded within the component identified as the "Baseband Procesor" (the PDCHarm2.x). The Baseband Processor includes both a receiving circuit and a transmitting circuit, as is more evident with reference to the detailed schematic reproduced as "Schematic 1" in Appendix A.

The transmitting circuit transmits a data signal in a given form to the transceiver.



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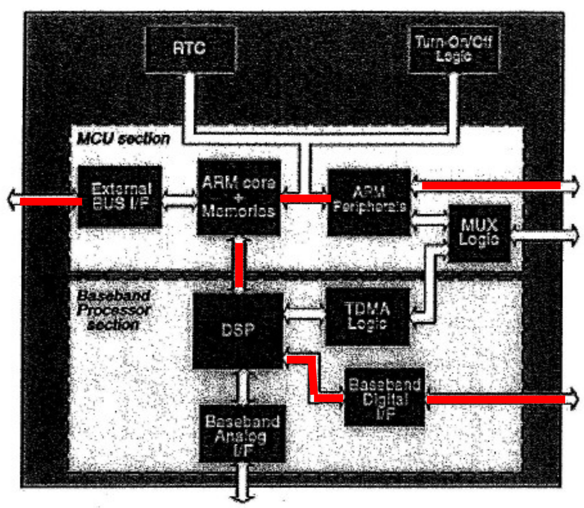
<td>a data bus to transfer one of said data signals between said device and the respective circuit,</td>
<td>The identified chipset component includes a data bus that operates to transfer data between the data transfer device and the receiving circuit, and to transfer data between the data transfer device and the transmitting circuit.



The data bus is at least partially contained within the integrated circuit forming the PDCharm2.x chip as a series of etched conductive paths or links between the functional blocks illustrated above in the chip. The data bus also further includes or couples to any of the memory buses, the general-purpose interface bus, the address/data microprocessor bus and other internal buses.</td>
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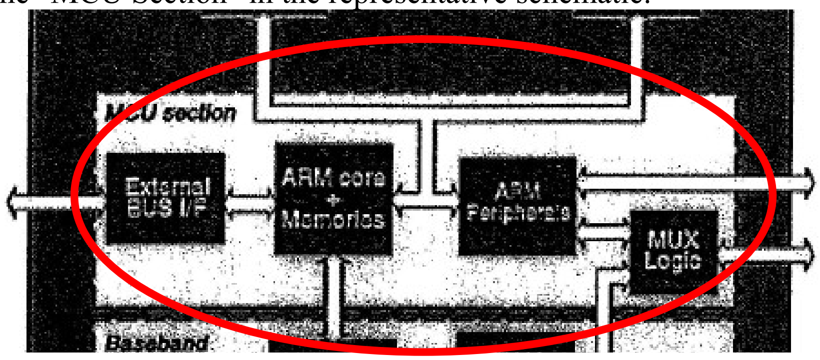
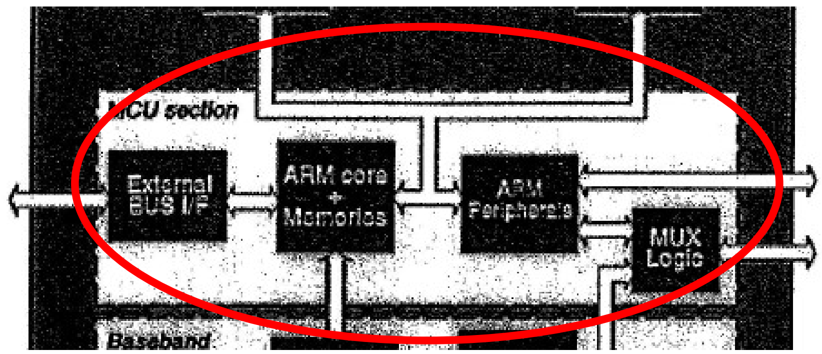
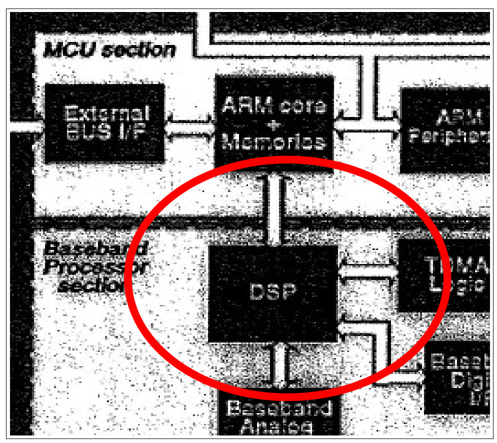
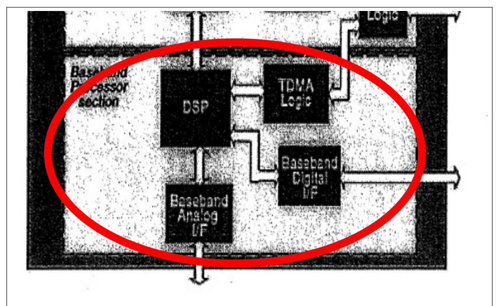
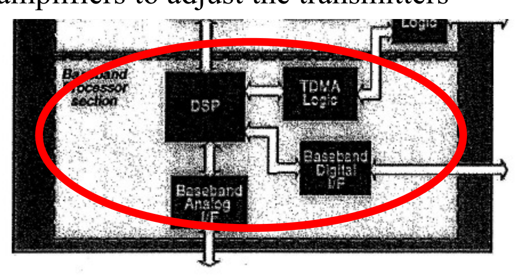
switch means to connect one of said circuits with said data bus	The accused instrumentalities include switch means that connect one of the receiving or transmitting circuits with the data bus. The identified chipset includes transistors and other logic gates for alternately coupling components of the chipset one to another for the purpose of isolating, blocking, routing and or conditioning of the data signals to connect the data bus with either of the receiving or transmitting circuits. The transistors and other logic gates may be implemented within the microprocessor or DSP identified as the "MCU Section" in the representative schematic.  The switch means comprises various logic gates and transistors that are in electrical cooperation with each of the various sub-components of the identified chip set that perform the function of the switch means. These various logic gates and transistors function to effectively connect the transmitting circuit or the receiving circuit to the data bus.
and **control means** to control said switch means,	The accused instrumentalities include electronic circuitry operable to control the switch means, to connect one of the transmitting or receiving circuits with the data bus. The control means is a microprocessor or digital signal processor (DSP) in the accused instrumentality executing code that provides logic for determining whether to connect one of the transmitting or receiving circuits with the data bus. The microprocessor under control of the source code is a special purpose machine including various logic gates and transistors, such as AND gates, flip-flops and inverters, that perform the function of the control means. The control means is illustrated below as the MCU section.

	The processors control the switching means to effectively connect the transmitting circuit and the receiving circuit to the data bus, to control the operation of the bus connection according to the intended destination of the signal to of from the data transfer device, to follow the change in the operational mode, to disconnect the connection in the unwanted route, and to maintain the effective connection in the wanted route. 
said control means being responsive to a signal from said data transfer device,	In the accused instrumentalities, the control means responds to a signal from any one or more of the data transfer devices. The signal comprises a change of state in one or more data bits that signals a change in the operational mode of the data transfer device and/or data ready to be transmitted or otherwise handled by the control means on behalf of the data transfer devices.
which is indicative of a change in the operational mode thereof	In the accused instrumentalities, the signal from the data transfer device consists of one or more bi-stable digital bits having states of logic "1" and logic "0" indicative of a change in operational mode respectively. A change from logic "0" to logic "1" or vice versa indicates a change in the operational mode of the data transfer device.
to disconnect said one circuit and connect the other of said circuits to said data bus.	In the accused instrumentalities, a change in logic state of the signal received from the data transfer device, results in the control means and switch means operatively terminating effective communication between one of the transmitting or receiving circuits over the data bus. Illustrated in Schematic 1 in Appendix A, the control means and the switch means operatively alternate modes of operation between transmission mode and receive mode, which causes the data transmission paths to alternate between the receiving circuitry and the transmitting circuitry.

2. An interface according to claim 1 wherein said signals are transferred between said data transfer device and said transceiver in serial form.	The accused instrumentalities include each of the elements specified by Claim 1. In addition, the data transfer devices included in the chip sets used in each accused instrumentality use a serial bus to transfer data with the transceiver. Accordingly, data are transferred between the data transfer device and the transceiver in serial form in the accused instrumentalities. Where the data transfer device is implemented as a component attached to a Universal Serial Bus (USB), the data signals are necessarily being transferred serially, which is an inherent feature of the Universal Serial Bus.
3. An interface according to claim 2 wherein said control means operates upon said transceiver to condition said transceiver to a transmit mode upon connection of said databus with said transmitting circuit.	The accused instrumentalities include each of the elements specified by Claim 2. In addition, the control means in the form of a microprocessor or digital signal processor, such as the DSP processor illustrated below, executing code functions to direct the transceiver to transmit when the control means and switch means operate to enable communication of data from the transmitting circuit to the transceiver over the data bus. 

4. An interface according to claim 2 wherein said control means is responsive to a change from an inactive to an active condition to connect said data bus to said transmitting circuit.	The accused instrumentalities include each of the elements specified by Claim 2. In addition, the control means in the form of a microprocessor executing code functions to enable data transfer from the data bus to the transmitting circuit when the user desires to communicate information. Such activation is indicated by a change in logic state in one or more logic bits within the microprocessor executing the code.
6. An interface according to claim 4 including amplifying means in said receiving circuit.	The RIM accused instrumentalities include each of the elements specified by Claim 4. The baseband circuits in the Baseband Processor section handle analog signals, therefore they must include integrated amplifiers. The amplifiers are designed for low-supply-voltage operations, and employ "push-pull" circuits at their output stages to achieve maximum available voltage swings and low signal distortions. 
7. An interface according to claim 6 wherein a buffer amplifier is included in said transmitting circuit to isolate said switch means and said transceiver.	The RIM accused instrumentalities include each of the elements specified by Claim 6. The baseband circuits in the Baseband Processor section handle analog signals, therefore they must include integrated amplifiers, which operate as buffer amplifiers to adjust the transmitters' modulation levels. The amplifiers are designed for low-supply-voltage operations, and employ "push-pull" circuits at their output stages to achieve maximum available voltage swings and low signal distortions. 

Appendix "A"

Representative Schematic Diagrams Reproduced from:

PDCharm2.x PDC Single-Chip Soulution Product Overview, Intel Corporation (unk.)

Schematic 1

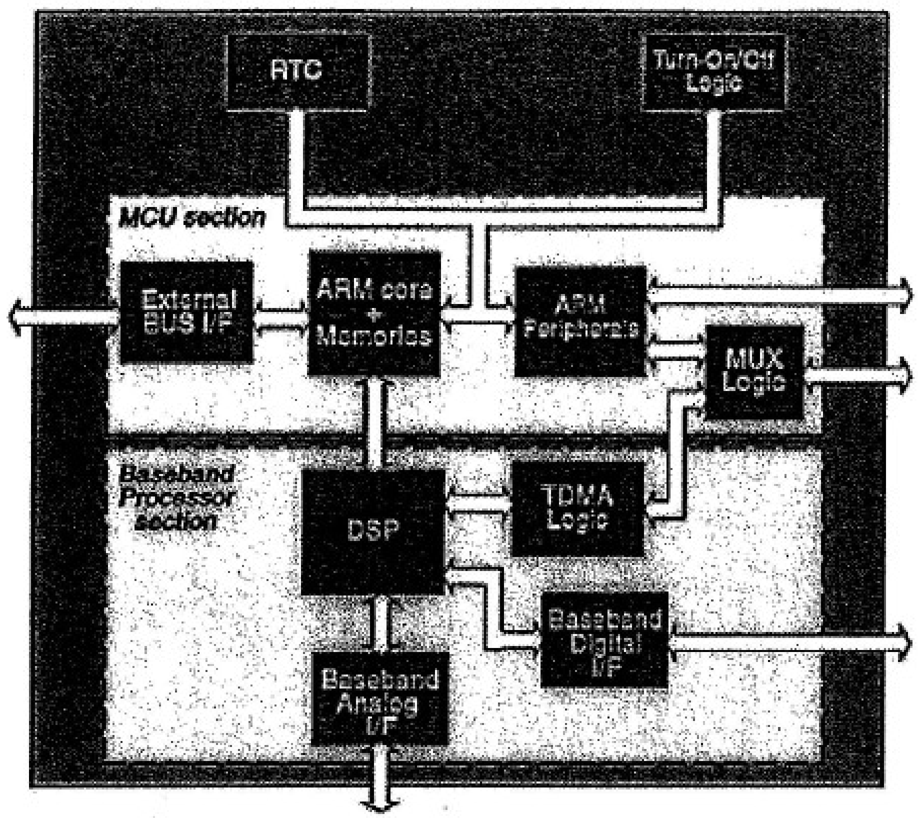


Figure 1: System Block Diagram of the PDCharm2.X

Schematic 2

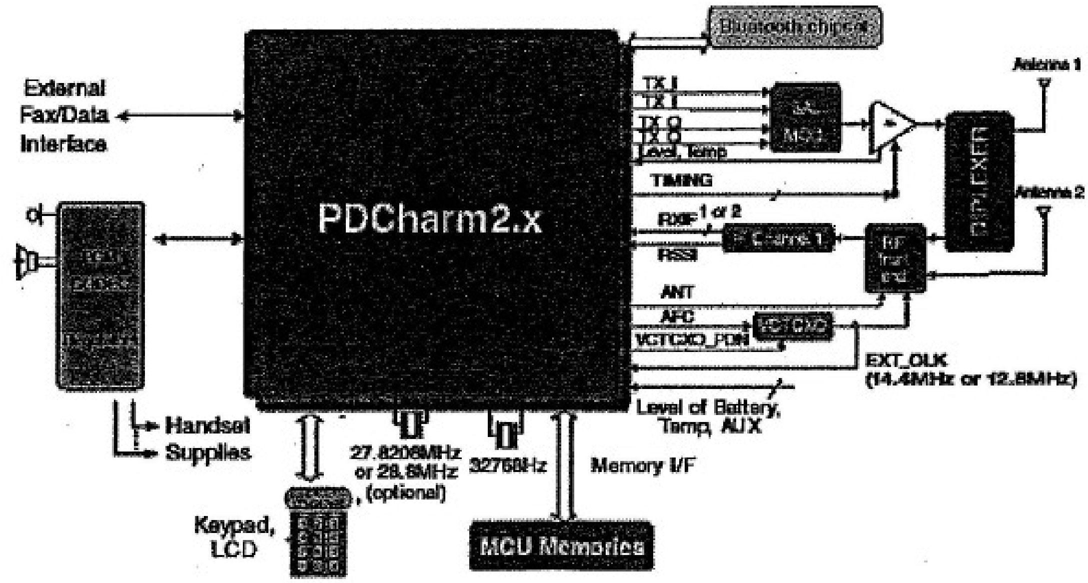


Figure 2: System Block Diagram of a typical handset design using PDCharm2.X